

REMARKS

This Amendment responds to the Office Action dated November 14, 2005 in which the Examiner rejected claims 1-2, 5-6 and 8 under 35 U.S.C. §103 and objected to the title.

As indicated above, a new title has been provided. Therefore, applicant respectfully requests the Examiner approves the new title.

Claim 1 claims a microcomputer comprising a memory, a central processing unit, and a functional block comprising a peripheral block, built-in the microcomputer. The memory has a reprogrammable nonvolatile memory storing user data, and in which a lock code is written in a specified area. The microcomputer comprises first and second decoding circuits and a logic circuit. The first decoding circuit is connected with the nonvolatile memory, which reads out the lock code, and decodes the lock code. The logic circuit performs a predetermined operation on an externally input mode bit, by the output from the first decoding circuit. The second decoding circuit decodes the processed mode bit by receiving the output from the logic circuit, and sends the obtained results to the functional block.

Through the structure of the claimed invention a) having a nonvolatile memory store user data and a lock code, b) having a first decoding circuit connected to the memory which stores user data and lock code and c) having a logic circuit perform an operation on an externally input mode bit, as claimed in claim 1, the claimed invention provides a microcomputer which cannot be arbitrarily accessed. The prior art does not show, teach or suggest the invention as claimed in claim 1.

Claim 5 claims a microcomputer comprising a memory, a central processing unit, a functional block comprising a peripheral block, built-in the microcomputer, and

an external terminal. The memory comprises a reprogrammable nonvolatile memory storing user data, and in which a function-selecting code for selecting the function of the external terminal is written in a specified area. The microcomputer comprises a first decoding circuit connected with the nonvolatile memory, which reads out the function-selecting code and decodes this code; and a selector circuit that selects a function of the external terminal by receiving the output from the first decoding circuit.

Through the structure of the claimed invention having a) a memory storing user data and a function-selecting code and b) a first decoding circuit connected to the memory storing the user data and code as claimed in claim 5, the claimed invention provides a microcomputer which can limit the function of an external terminal. The prior art does not show, teach or suggest the invention as claimed in claim 5.

Claim 6 claims a microcomputer comprising a memory, a central processing unit, and a functional block comprising a peripheral block, built-in the microcomputer. The memory comprises a reprogrammable nonvolatile memory storing user data, and in which a limiting code for limiting a command is written in a specified area. The microcomputer comprises a first decoding circuit connected with the nonvolatile memory, which reads out the limiting code, and decodes this code; and a second decoding circuit that limits a command to be used, by the output from the first decoding circuit.

Through the structure of the claimed invention a) having a memory storing user data and a limiting code and b) having a first decoding unit connected to the memory as claimed in claim 6, the claimed invention provides a microcomputer

which can prevent false writings and intentional reprogramming by users. The prior art does not show, teach or suggest the invention as claimed in claim 6.

Claims 1-2, 5-6 and 8 were rejected under 35 U.S.C. §103 as being unpatentable over *Sibigtroth et al* (U.S. Patent No. 5,251,304) and Official Notice.

Applicant respectfully traverses the Examiner's rejection of the claims under 35 U.S.C. §103. The claims have been reviewed in light of the Office Action, and for reasons which will be set forth below, Applicant respectfully requests the Examiner withdraws the rejection to the claims and allows the claims to issue.

Sibigtroth et al appears to disclose security of information stored in memory used by data processors. (col. 1, lines 10-11) Shown in FIG. 1 is a block diagram of a data processing system 10, comprised generally of a single integrated circuit package portion 11 and a peripheral portion 12 having an external peripheral device. The integrated circuit package portion 11 has a memory 13, a data processor 14, a decoder 16, an instruction inhibit circuit 18, and a programmable security device 20. (col. 2, lines 18-25) In operation, system 10 of FIG. 1 is generally operating in one of three modes. The first of the three operational modes is a "single chip mode". The single chip mode of operation requires data processor 14 to address predetermined memory locations of memory 13 via address bus 22 for the purpose of either reading instructions and data from memory 13 or writing data to memory 13. A second mode of operation of system 10 is an "expanded mode". In the expanded mode of operation, data/instruction bus 30 is coupled to data/instruction bus 24 by the instruction inhibit circuit 18, which is effectively transparent in expanded mode operation. In the expanded mode of operation, data processor 14 can access either memory 13 or peripheral portion 12 for both instructions and data. Since expanded

mode operation allows data processor 14 to read instructions from peripheral portion 12, the instructions presented to data processor 14 via data/instruction buses 24 or 30, may be readily observed or interrupted for the purpose of reading or modifying the contents of memory 13; therefore the expanded mode of operation is not secure. A third mode of operation of system 10 is a "secure mode". The secure mode of operation affects the interaction of memory 13, data processor 14, decoder 16, programmable security device 20, address bus 22, data/instruction buses 24 and 30, and control buses 26 and 28 which are contained within integrated circuit package portion 11 and peripheral portion 12 contained within data processing system 10. Illustrated in FIG. 2 is a logic diagram of the instruction inhibit circuit 18 of FIG. 1 and generally comprising an inverter 50, an AND gate 52, an OR gate 54 and one or more pair of isolation buffers such as an isolation buffer pair 56 comprising buffers 58 and 60. An input of inverter 50 receives the Enable signal from programmable security device 20 of FIG. 1. A first input of AND gate 52 is connected to an output of inverter 50, and a second input of AND gate 52 is connected to the Instruction Fetch signal of decoder 16 of FIG. 1. A first input of OR gate 54 is connected to an output of AND gate 52, and a second input of OR gate 54 is connected to the Data Read signal contained within control bus 26 of FIG. 1. An output of OR gate 54 provides an output signal labeled "Read Instruction/Data". Each isolation buffer pair, such as buffers 58 and 60, has a first control input for receiving the Read Instruction/Data signal and a second control input for receiving the Data Write signal. Each isolation buffer pair is connected to data/instruction bus 30 and data/instruction bus 24 of FIG. 1. In the illustrated form, an active signal is a logic high signal. The Enable signal provided by programmable security device 20 is activated when the data

processing system 10 of FIG. 1 is to operate in the secure mode in response to the Control signal. Programmable security device 20 may be implemented as any type of nonvolatile storage device meaning that the state of the Enable signal remains valid even if power is removed from data processing system 10. Therefore, in one form programmable security device 20 may be implemented with a nonvolatile memory. (col. 3, line 1 through col. 4, line 6)

Applicant respectfully traverses the Examiner's statement that storing user data on a non-volatile memory in addition to enable code is an obvious variation. *Sibigtroth et al.* merely discloses storing a state of an enable signal. The Examiner goes on to state that reconfigurable non-volatile memories are well known in the art. Applicants respectfully submit that the issue is not whether the invention can be modified in light of the prior art. Rather, patentability hinges upon whether there is any teaching to modify the prior art to arrive at the claimed invention. Nothing in *Sibigtroth et al.* shows, teaches or suggests storing anything other than an enable signal. Nothing in the Official Notice shows, teaches or suggests why it would be obvious to modify *Sibigtroth et al.* to store anything other than an enable signal and in particular store user data and one of a lock code, function-selecting code or limiting code as claimed in claims 1, 5 and 6. Applicant respectfully submits that there is no teaching in either *Sibigtroth et al.* or the Official Notice which would lead a person of ordinary skill in the art to store user data and one of a lock code, function-selecting code or limiting code as claimed in claims 1, 5 and 6.

Additionally, Applicants respectfully traverse the Examiner's statement that since the instruction Fetch signal in Figure 1 is output from decoder 16 and input to instruction inhibit 16, it is inherent that it is external to the instructions inhibit circuit

18 and is an external input mode bit. Applicants respectfully bring the Examiner's attention to column 2, lines 19-25 of *Sibigtroth et al.* which states that the data processor system 10 comprises a single integrated circuit package portion 11 and a peripheral portion 12 having an external peripheral device. Additionally, the circuit package portion 11 includes memory 13, data processor 14, decoder 16, instruction inhibit circuit 18 and programmable security device 20. Thus *Sibigtroth et al.* clearly discloses that the instructions inhibit circuit 18 and decoder 16 are internal to the integrated circuit package portion 11 while external periphery portion 12 is external to the package 11. Therefore, Applicant respectfully submits that the Fetch signal from decoder 16 is an internal signal to the circuit package 11 and is not an external input mode bit as claimed in claim 1. Rather, *Sibigtroth et al.* teaches away from the claimed invention since the decoder 16 and instruction inhibit circuit 18 are provided in the same single integrated circuit package portion 11 and therefore the instruction Fetch signal output by the decoder 16 is an internal signal.

Since nothing in *Sibigtroth et al* and Official Notice shows, teaches or suggests a) a memory storing user data and a code and a first decoding circuit connected with the memory which reads out the code as claimed in claims 1, 5 and 6, and b) a logic circuit that performs a predetermined operation on an externally input bit mode as claimed in claim 1, applicant respectfully requests the Examiner withdraws the rejection to claims 1, 5 and 6 under 35 U.S.C. §103.

Claims 2 and 8 recite additional features. Applicant respectfully submits that claims 2 and 8 would not have been unpatentable over *Sibigtroth et al* and Official Notice within the meaning of 35 U.S.C. §103 at least for the reasons as set forth

above. Therefore, applicant respectfully requests the Examiner withdraws the rejection to claims 2 and 8 under 35 U.S.C. §103.

Thus it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested. Should the Examiner find that the application is not now in condition for allowance, Applicant respectfully requests the Examiner enters this response for purposes of appeal.

If for any reason the Examiner feels that the application is not now in condition for allowance, the Examiner is requested to contact, by telephone, the Applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, Applicant respectfully petitions for an appropriate extension of time. The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

BUCHANAN INGERSOLL PC

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